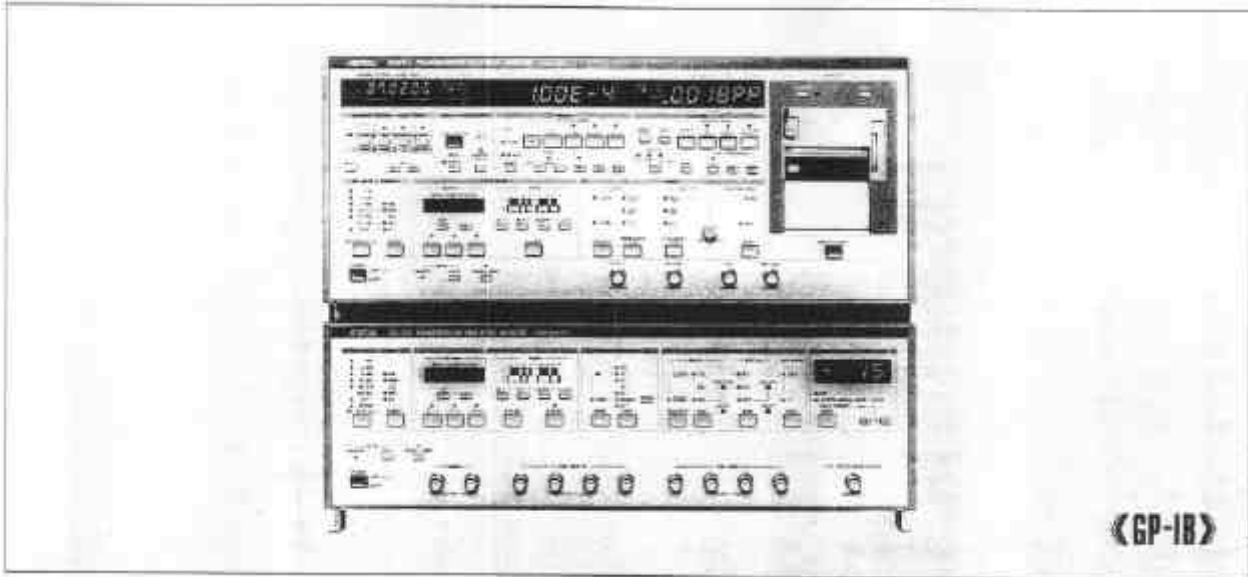


PCM MEASURING INSTRUMENTS

DIGITAL TRANSMISSION ANALYZER ME520B

1 kHz to 150 MHz, 1 kHz to 170 MHz (with Option 02)



The ME520B is used to measure error rate and jitter of PCM signals with clock frequencies ranging from 1 kHz to 150 MHz (in which 1st to 4th order PCM hierarchy and 10 CH system are included).

It is possible to measure error rate and jitter simultaneously. Measured data are indicated on a digital display and analyzed at the same time. The analysis results, in combination with time/date, are printed out by an internal printer, thus, continuous measurement for long periods is possible.

The ME520B is best suited for development and maintenance of radio PCM, wired PCM, optical fiber systems or other digital communication systems.

Its transmitter and receiver are housed in separate cabinets, making end-to-end measurement possible. The transmitter generates M-sequence pseudorandom pattern signals and jitter modulated signals that are close to actual transmitted signals. The receiver receives signals from the system under measurement and detects error and the amount of jitter. Furthermore, the ME520B can perform error analysis in accordance with the CCITT Rec. G.821, so the ME520B is indispensable for evaluation of international communication circuits.

Features

- Conforms to CCITT Recommendations
- Simultaneous measurement of error and jitter
- End-to-end measurement
- A variety of test patterns enable testing digital systems including PCM transmission over cables, radio and optical fiber links
 - CMI pattern : 4 outputs
 - Bipolar pattern : 4 outputs
 - AMI, HDB3 code
 - Unipolar pattern : 4 outputs
 - Clock : 2 outputs
- Measuring pattern
 - Pseudorandom : $2^{10}-1, 2^{15}-1, 2^{23}-1$ bits
 - Word pattern : Programmable 16 bits or 2×8 bits word
- Error addition
 - Bit or code errors with $10^{-3}, 10^{-4}, 10^{-5}$ or 10^{-6} error rate or single error can be added to the sending pattern.
- Zero substitution
 - The sequence can be disabled for 8 to 120 clock periods.
- Code error measurement is possible for actual line in service

Specifications

• Transmitter

Bit rate	Internal clock	Bit rate	704, 2048, 6448, 34368, 68736, 139264 kbit/s	
		Accuracy	± 2 ppm, ± 5 ppm/ $^{\circ}$ C to 50° C	
	External clock	Frequency	1 kHz to 150 MHz, (Option 02 up to 170 MHz)	
		Amplitude	0.3 to 3 Vp-p, 1 kHz to 1 MHz (rectangular), > 1 MHz (Sine or rectangular)	
		Impedance	Nominal 75 Ω , unbalanced	
		Duty cycle	50%	
Clock output	Numbers	2 separate buffered outputs, common phase		
	Polarity	CLOCK or $\overline{\text{CLOCK}}$, selectable		
	Level	TTL	High state ≈ 2.5 V, low state ≈ 0.5 V	
		ECL	ECL level	
		SET	Amplitude 1 to 2 V, offset 0 to ± 2 V	
	Format	Square wave, 50% $\pm 10\%$ duty cycle on internal clock		
Impedance	75 Ω , unbalanced			

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Pattern	PRBS (Pseudorandom binary sequence)	$2^{10} - 1, 2^{15} - 1, 2^{23} - 1$	
	Word	Freely programmable digital word, adjustable length 1 to 16 bits Two 8-bit words, any possible setting (Can be changed over by an external control signal)	
	Zero substitution	Sequence can be disabled for 8 to 120 of clock periods, in multiples of 8 clock periods.	
Error pulse	Error addition	Error rate	$10^{-3}, 10^{-4}, 10^{-5}$ and 10^{-6} , selectable
		Single error	1 error is produced for each depression of key
	External error input	Impedance	Nominal 680 Ω , unbalanced to -5.2 V
		Frequency	DC to one-fourth of the clock frequency
Output data	CMI	Bit rate	1 kbit/s to 150 Mbit/s, 1 kbit/s to 170 Mbit/s (Option 02)
		Amplitude	1 ± 0.1 Vp-p
		Numbers	4 separate buffered outputs, common phase
	Unipolar (RZ, NRZ)	Bit rate	1 kbit/s to 150 Mbit/s, (Option 02: up to 170 MHz)
		Level	TTL, ECL, SET, selectable [TTL: high state ≈ 2.5 V, low state ≈ 0.5 V] [SET: amplitude 1 to 2 V, offset 0 to ± 2 V]
		RZ duty cycle	50% $\pm 10\%$ on internal clock
		NRZ width	100% $\pm 5\%$
		Numbers	4 separate buffered outputs, each delayed 4 bits
	Bipolar (RZ)	Bit rate	1 kbit/s to 50 Mbit/s
		Format	AMI, HDB3
Amplitude		2.37 ± 0.237 V/0 ± 0.237 V or 1.0 ± 0.1 V/0 ± 0.1 V, selectable	
Numbers		4 separate buffered outputs, each delayed 4 bits	
Jitter modulation	Function	Timing jitter can be added to the clock and data output signals by applying an external modulation source	
	Input	Frequency	DC to 5% or 2.5% of bit rate (see Fig. 1 and Table 1)
		Sensitivity	10 Ulp-p/V (5 Hz)
		Impedance	Nominal 75 Ω , unbalanced to ground
	Output	Display	10.10 Ulp-p, max.
Jitter reference clock output	Level	ECL	
	Impedance	Nominal low unbalanced to ground	
Pattern sync output	Pattern	PRBS	1 pulse/sequence
		2 to 16 bits word length	1 pulse/2 sequences
		1 bit word length	1 pulse/4 bits
		2 x 8-bit word length	1 pulse/sequence
GP-IB interface	Meets IEEE Standard 488-1978		
Ambient temperature, rated range of use	0° to 50°C		
Power	AC 90 to 138 V or AC 180 to 275 V, 50/60 Hz, approx. 200 VA		
Dimensions and weight	132.5H x 426W x 351D mm, approx. 11 kg		

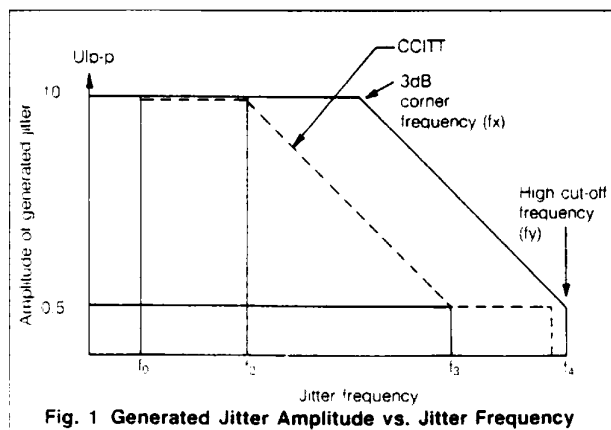


Table 1 Jitter frequency

Bit rate (kb/s)	CCITT Rec. O.171				ME520B	
	f_0 (Hz)	f_2 (kHz)	f_3 (kHz)	f_4 (kHz)	f_x^* (kHz)	f_y^* (kHz)
704	—	—	—	—	4.5	35
2,048	2	2.4	45	100	13	102
8,448	2	10.7	200	400	50	422
34,368	2	1.0	20	800	210	1,000
68,736	—	—	—	—	300	2,000
139,264	2	0.5	10	3,500	600	4,000
EXT	Can be modulated at internal rates $\pm 10\%$					

*Typical figures

Note: When used in conjunction with the MH370A Jitter Modulation Oscillator, the ME520B can perform the maximum input jitter tolerance test according to the CCITT Rec. G. 703. For details, please refer to the MH370A data sheet.

PCM MEASURING INSTRUMENTS

• Receiver

Bit rate	Clock recovery	Receiving rate	704, 2048, 8448, 34368, 68736, 139264 kbit/s	
		Pulling range	± 50 ppm (Jitter measurement), ± 100 ppm (AMI), $\pm 3\%$ (HDB3), $\pm 1\%$ (68736 kbit/s CMI), $\pm 3\%$ (139264 kbit/s CMI)	
		Format	AMI, HDB3 (704, 2048, 8448, 34368 kbit/s), CMI (68736, 139264 kbit/s)	
	Clock input	Polarity	CLOCK or $\overline{\text{CLOCK}}$, selectable	
		Frequency	1 kHz to 150 MHz (Option 02 up to 170 MHz)	
		Amplitude	0.3 to 3 V _{p-p}	
		Impedance	75 Ω , unbalanced	
	Termination	Ground or nominal - 2 V (via switch)		
Pattern	PRBS (Pseudorandom binary sequence)	$2^{10} - 1$, $2^{15} - 1$, $2^{23} - 1$		
	Word	Freely programmable digital word, adjustable length 1 to 16 bits		
	Zero substitution	Sequence can be disabled for 8 to 120 of clock periods, in multiples of 8 clock periods		
Input data	RZ, NRZ input	Bit rate	1 kbit/s to 150 Mbit/s, (Option 02 up to 170 MHz)	
		Threshold	-3 V to +3 V, ground or ECL, selectable	
		Impedance	75 Ω , unbalanced	
		Amplitude	0.3 to 3 V _{p-p}	
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level	
	CMI input	Threshold	Ground	
		Impedance	75 Ω , unbalanced	
		Amplitude	1 V _{p-p} automatic \sqrt{f} equalization	
		Monitor mode	Additional gain 26 to 30 dB	
	AMI, HDB3 input	Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level	
		Impedance	75 Ω , unbalanced	
		Amplitude	2.37 V _{IO} V (704, 2048, 8448 kbit/s), 1 V _{IO} V (34368 kbit/s), Automatic \sqrt{f} equalization	
		Monitor mode	Additional gain at 30 dB: 704, 2048, 8448 kbit/s Additional gain at 26 dB: 34368 kbit/s	
	Error measurement	Bit error		Closed loop bit-by-bit detection at the binary level
		Code error	AMI	Bipolar violations are code errors
HDB3			"Violation of violations" rule, i.e., two consecutive bipolar violations with same polarity	
CMI			"Violation of CMI coding rules", i.e., two consecutive bits, whose intervals are one full unit time with same polarity	
Block error			For PRBS only, the block length coincides with the length of the PRBS Error is detected if a block contains one or more bit errors	
Pattern synchronization		Mode		Automatic or manual
		Sync gain		PRBS: No errors in 32 clock periods WORD: No errors in 32 to 512 clock periods
	Sync loss		PRBS: Approx. 10,000 errors in 30,000 clock periods WORD: Approx. 1,000 errors in 30,000 clock periods	
Error display	Error rate	Display	0.00E-MN (0.00 $\times 10^{\text{MN}}$), MN = 1 to 15 with automatic scaling	
		Accuracy	Indication given if measurement result is based on < 100 errors	
	Error count	Method		Totalizes errors over selected gating period
		Display		6-digit LED display with leading zero blanking When count exceeds 999999, display automatically changes to 0.00E00, with automatic round-up to a maximum count of 9.99E15 (9.99 $\times 10^{15}$)
	Error intervals	Method		Totalizes the number of intervals (1.0 to 0.01 s) which contain one or more errors (Intervals can be selected by the switch on rear panel)
		Display		Same as error count
	Error-free intervals %	Method		Totalizes the number of intervals (1.0 to 0.01 s) during which no errors occur over selected gating period
		Display		6-digit LED display with leading zero blanking up to 100.000%

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Error performance display	%US (% unavailable second)		Displays % values including 4 digits of decimal part Error rate threshold: 1×10^{-2} to 1×10^{-4} Error count threshold: 1 to 999999, 1.00×10^6 to 1.99×10^7	
	%SES (% severely errored second)		Error rate averaged per 1 second or the total number of 1 second intervals exceeding threshold. Displays % values including 4 digits of decimal part Error rate threshold: 1×10^{-2} to 1×10^{-4} Error count threshold: 1 to 999999, 1.00×10^6 to 1.99×10^7	
	%DM (% degraded minutes)		Error rate averaged per 1 second or rate of time in which 1 minute error count exceeded threshold. Displays % values including 4 digits of decimal part Error rate threshold: 1×10^{-5} to 1×10^{-7} Error count threshold: 1 to 999999, 1.00×10^6 to 1.99×10^8	
	%ES (% errored second)		The total number of 1 second intervals containing at least one count error Displays % values including 4 digits of decimal part	
Status display	Display		Live and last record of no signal, sync loss, AIS, < 100 errors	
Jitter measurement	Range, accuracy	1 UI	0.000 to 1 010 UIp-p	
		10 UI	0.00 to 10 10 UIp-p, $\pm 4\%$ \pm additional error as shown in Table 2 (with HP1, LP)	
	Jitter amplitude versus jitter frequency		Refer to Fig. 2 and Table 3	
	Hit count	Display	When count exceeds 999999, display automatically changes to 0 00E00, with automatic round-up to a maximum count of 9 99E15 (9.99×10^{15}).	
		Sensitivity	Typically ≥ 100 ns pulse width counted	
		Hit threshold	Range 1: 0.05 to 0.5 UIp-p Range 10: 0.5 to 5.0 UIp-p	
		Accuracy	Typically $\pm 5\%$	
	Hit intervals	Method	Totalizes the number of hit intervals (1, 0.1, 0.01 s). Intervals can be selected by the switch.	
		Other specifications are same as hit count.		
Hit-free intervals %	Method	Totalizes the number of intervals (1, 0.1, 0.01 s) during which no hits occur		
	Display	6-digit LED display with leading zero blanking up to 100 000%		
Gating period and real time clock	Gating period	Setting	Manual, clock, time	
		Display	Last data	Displayed data and status record is data in last gating period.
	Current data		Displayed data and status record is data in current gating period.	
Real-time clock	Year, month, day, hour, minute, second			
GP-IB interface	Meets IEEE Standard 488-1978			
Ambient temperature, rated range of use	0° to 50°C			
Power	AC 90 to 138/180 to 250 V, 50/60 Hz, approx. 230 VA			
Dimensions and weight	177H x 426W x 351D mm, approx. 15 kg			

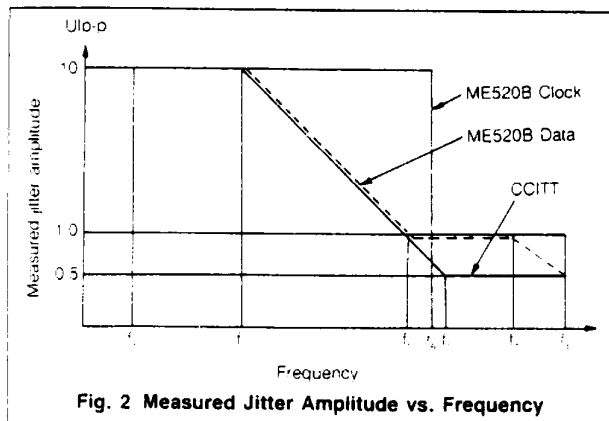


Table 2 Jitter Frequency

Bit rate (kbit/s)	CCITT Rec. O.171				ME520B (typical)		
	f_1 (Hz)	f_2 (Hz)	f_3 (Hz)	f_4 (Hz)	f_5 (Hz)	f_6 (Hz)	f_7 (Hz)
704	(20)	(1 k)		(35 k)	7	8 k	10 k
2 048	20	2.4 k	45 k	100 k	24	27 k	30 k
8 448	20	10.7 k	200 k	400 k	107	110 k	120 k
34 368	100	1 k	20 k	800 k	10	344 k	320 k
68 736	(100)	(40 k)	—	(1 M)	400	400 k	500 k
139 264	200	500	10 k	3.5 M	100	500 k	1.4 M

Table 3 Additional Error

Range	Additional error in UIp-p				
	Data		Clock		
	HDB3	CMI*	$f \leq 50$ M	50 M < $f \leq 150$ M	$f > 150$ M (OPT 02)
1 UIp-p	≤ 0.035	≤ 0.08	≤ 0.01	≤ 0.02	≤ 0.03
10 UIp-p	≤ 0.12	≤ 0.24	≤ 0.1	≤ 0.2	≤ 0.3

*The residual jitter of 139264 kbit/s CMI signals can be improved by using the MH547A Clock Recovery.